In the Claims:

1. (Previously Presented) A multi-issue processor comprising:

a register file; and

a plurality of issue slots, each one of the plurality of issue slots including

a plurality of functional units,

an input routing network that provides multiple data path outputs for a single data path input, the input routing network receiving data from the register file on the single data path input via a single data input path and providing data from the register file to functional units of the plurality of functional units, the data provided on the multiple data path outputs via multiple data output paths, and

a plurality of holdable registers that hold duplicate data from the register file,

wherein in a first set of the plurality of issue slots the holdable registers store data on the multiple data output paths of the first set and the holdable registers in the first set do not store data on the single data input path corresponding to the input routing networks of the first set and in a second set of the plurality of issue slots the holdable registers store data on the single data input path corresponding to the input routing networks of the second set and the holdable registers in the second set do not store data on the multiple data output paths of the second set.

2. (Previously Presented) A multi-issue processor according to Claim 1, wherein

a first instruction set accesses at least the first set of issue slots; and

a second instruction set accesses the second set of issue slots.

3. (Currently amended) A multi-issue processor according to Claim 1, wherein

the input routing network of each of the plurality of issue slots has a plurality of data path inputs; and

in the second set of issue slots holdable registers of the plurality of holdable registers are located between each of the inputs of the input routing network and the register file.

4. (Previously Presented) A multi-issue processor according to Claim 1, wherein, in the first set of issue slots, holdable registers are located between the input routing networks and each of the plurality of function units.

5. (Previously Presented) A multi-issue processor according to Claim 1, wherein the first set of issue slots are accessed by a first set of instructions for a very-large-instruction-word (VLIW) processor and the second set of issue slots are accessed by a second set of instructions that are used by an interrupt routine.

6. (Previously Presented) A multi-issue processor according to Claim 5, wherein the second set of instructions has less instructions than the first set of instructions.

7. (Previously Presented) A multi-issue processor according to Claim 1, wherein the first set of issue slots has more issue slots than the second set of issue slots.

8. (Previously Presented) A circuit for use in a computing system having at least one multi-issue processor, with

a register file; and

a plurality of issue slots, each one of the plurality of issue slots including

an input routing network that provides multiple data path outputs for a single data path input, the input routing network receiving data from the register file on the single data path input via a single data input path and providing data from the register file to outputs of functional units, the data provided on the multiple data path outputs via multiple data output paths, and

the circuit comprising:

a plurality of holdable registers that hold duplicate data from the register file, wherein in a first set of the plurality of issue slots the holdable registers store data on the multiple data output paths of the first set and the holdable registers in the first set do not store data on the single data input path corresponding to the input routing networks of the first set and in a second set of the plurality of issue slots the holdable registers store data on the single data input path corresponding to the input routing networks of the second set

and the holdable registers in the second set do not store data on the multiple data output paths of the second set.

9. (Previously Presented) The circuit of claim 8, wherein

a first instruction set accesses at least the first set of issue slots; and

a second instruction set accesses the second set of issue slots.

10. (Previously Presented) The circuit of claim 8, wherein, in the first set of issue slots, holdable registers are located between the input routing networks and each of the plurality of function units.

11. (Previously Presented) The circuit of claim 8, wherein the second set of instructions has less instructions than the first set of instructions.

12. (Previously Presented) The circuit of claim 8, wherein the first set of issue slots has more issue slots than the second set of issue slots.

13. (New) A multi-issue processor comprising:

a register file;

a first set of one or more issue slots, each issue slot including:

a plurality of functional units, the issue slot configured to reduce power usage by preventing switching of combinatorial gates in each respective one of the plurality of functional units during clock cycles when the functional unit is not in use; and

an input routing network having an input path coupled to the register file and having a plurality of output paths coupled to respective ones of the plurality of functional units;

a second set of one or more issue slots, each issue slot including:

a plurality of functional units;

an input routing network having an input path coupled to the register file and having a plurality of output paths coupled to respective ones of the plurality of

functional units, the input path including a register coupled to store data on the input path and the output paths not including registers for data storage; and

a controller circuit for controlling which issue slots of the first and second sets of one or more issue slots are used to process respective instructions received by the multi-issue processor, the controller circuit configured to:

in response to determining respective instructions received by the multi issue processor are included in a first instruction set, process the instructions using one or more of at least the first set of one or more issue slots; and

in response to determining respective instructions received by the multi issue processor are included in a second instruction set, process the instructions using only one or more of the second set of one or more issue slots.

14. (New) The multi-issue processor of claim 13, wherein the multi-issue processor is configured to execute an interrupt service routine, consisting of one or more instructions included in the second instruction set, in response to an interrupt signal.

15. (New) The multi-issue processor of claim 14, wherein in response to the interrupt signal, the multi-issue processor is further configured to:

retrieve a data value from the register of the one of the second set of one or more issue slots;

execute the interrupt service routine using only one or more of the functional units of the one of the second set of one or more issue slots; and

restore the register of the one of the second set of one or more issue slots to the retrieved data value.

16. (New) The multi-issue processor of claim 13, wherein each issue slot in the first set of one or more issue slots:

includes a holdable register on the respective output path coupled to each of the plurality of functional units; and

is configured to prevent switching of combinatorial gates of each respective one of the plurality of functional units by disabling the holdable register on the corresponding output path coupled to the respective one of the plurality of functional units.

17. (New) A multi-issue processor of claim 13, wherein for each of the second set of issue slots the input routing network includes at least a second input path coupled to the instruction register, the at least one other input path each including a register coupled to store data on the at least second input path.